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| 10/715,064 | 11/17/2003 | **Anand Pande** | 15156US01 | 7036 |

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| EXAMINER | |
|---|---|
| TSAI, SHENG JEN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/715,064 | PANDE, ANAND | |
| | Examiner | Art Unit | |
| | SHENG-JEN TSAI | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

**1**. This Office Action is taken in response to Applicant's Remarks filed on January 15, 2008 regarding application 10/715,064 filed on November 17, 2003.

**2**. Claims 1-6 have been cancelled previously.

Claims 7-11 are pending for consideration.

**3**. ***Response to Remarks***

Applicants' amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Applicant contend that the Castellano reference teaches away from using a "conventional sequential counters" because "bogus values may be obtained," thus it is improper to modify Castellano's scheme in view of Kao's invention to have a "Gray to binary converter for generating address." The Examiner disagrees.

Castellano's comment on "bogus values may be obtained" applies when only a "conventional sequential counters," or a "binary counter," is used directly to generate addresses.

However, as demonstrated by Kao's invention, the modification on Castellano's scheme is to use a "Gray to binary converter," instead of a "binary counter" directly, to generate addresses. Since the problem of multiple bits changing values is resolved by using the Grey counter as the first stage, the bogus values are eliminated. Thus a conventional linear address space can be obtained without the bogus values by using a "Gray to binary converter."

Therefore, the Examiner's position regarding the patentability of claims 7-11 remains the same as stated in the previous Office Action.

***Claim Rejections - 35 USC § 103***

**4**. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5**. Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Castellano (US 5,555,524), and in view of Kao et al. (US 6,263,410, hereinafter referred to as Kao).

As to claim 7, Castellano discloses **a circuit for storing data** [figures 1-2 show the details of the circuit], **said circuit comprising**:

**a FIFO for queuing the data** [An FIFO is provided which has two synchronous ports that may operate asynchronously to one another … (abstract); figure 1, 10; column 3, lines 3-8];

**a read pointer for indicating a particular address in the FIFO** [Read Address (RA), figure 1, 6; column 3, lines 16-23];

**a write pointer for indicating another particular address in the FIFO** [Write Address (WA), figure 1, 6; column 3, lines 8-15];

**a first Gray code to binary converter for generating the particular address indicated by the read pointer** [taught by Kao, see below];

**a second Gray code to binary converter for generating the particular address indicated by the write pointer** [taught by Kao, see below]**; and**

**a comparator** [EMPTY indicator circuit, figure e1, 30, and FULL indicator circuit, figure 1, 40] **for determining whether the FIFO is empty** [EMPTY, figure 1, 31] **or full** [FULL, figure 1, 41] **based on a comparison of a Gray code associated with the read pointer and a Gray code associated with the write pointer** [figure 1 shows that the EMPTY and FULL indicator circuits are based on signals RA and WA, which are Gray coded read and write address signals, respectively, as shown in figure 1, 20 and 18].

Regarding claim 7, Castellano does not teach **a first Gray code to binary converter for generating the particular address indicated by the read pointer** or **a second Gray code to binary converter for generating the particular address indicated by the write pointer.**

Kao teaches in the invention "Apparatus and Method for Asynchronous Dual Port FIFO" a FIFO based circuit with Gray code in which a first Gray code to binary converter for generating the particular address indicated by the read pointer [Gray Code to Sequential Converter, figure 9] and a second Gray code to binary converter for generating the particular address indicated by the write pointer [Gray Code to Sequential Converter, figure 3, 306]**.**

Sequential addresses are most suitable when sequential data is to be stored in consecutive addresses in the FIFO, because the addressing schemes used by computer systems are mostly based on a linear, continuous address assignment.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to use a first Gray code to binary converter for generating the particular address indicated by the read pointer and a second Gray code to binary converter for generating the particular address indicated by the write pointer, as demonstrated by Kao, and to incorporate it into the existing apparatus disclosed by Castellano, to support a linear, continuous address scheme employed by most of the computer systems.

As to claim 8, Castellano teaches that **a first Gray code generator for generating the Gray code associated with the read pointer** [the Read Gray Counter, figure 1, 20]**; and**

**a second Gray code generator for generating the Gray code associated with the write pointer** [the Write Gray Counter, figure 1, 18].

As to claim 9, Kao teaches that **a first Gray code to binary converter for generating the particular address indicated by the read pointer** [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code]**; and**

**a second Gray code to binary converter for generating the another particular address indicated by the write pointer** [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code];

**wherein the first Gray code to binary converter receives the Gray code associated with the read pointer from the first Gray code generator** [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code]**; and**

**wherein the second Gray code to binary converter receives the Gray code associated with the write pointer from the second Gray code generator** [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code].

As to claim 10, Castellano teaches that **the FIFO comprises a FIFO RAM** [dual port RAM FIFO, figure 1, 12; column 3, lines 3-8].

As to claim 11, it recites substantially the same limitations as in claim 7, and is rejected for the same reasons set forth in the analysis of claim 7. Refer to "As to claim 7" presented earlier in this Office Action for details.

**6.** ***Related Prior Art Of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Hsu et al., (US 6,845,414), "Apparatus and Method of Asynchronous FIFO Control."

- Camilleri et al., (US 6,434,642), "FIFO Memory System and Method with Improved Determination of Full and Empty Conditions and Amount of Data Stored."
- Shyi et al., (US 5,426,756), "Memory Controller and Method Determining Empty/Full Status of a FIFO Memory Using Gray Code Counters."
- Brooks et al., (US 5,410,664), "RAM Addressing Apparatus with Lower Power Consumption and Less Noise Generation."
- Cohn et al., (US 4,556,960), "Address Sequencer for Overwrite Avoidance."
- Jiang, (US Patent Application Publication 2004/0207547), "Method of Scalable Gray Coding."
- Pontius, (US 6,337,893), "Non-Power-Of-Two Gray-Code Counter System Having Binary Incrementer with Counts Distributed with Bilateral Symmetry."
- Yi, (US 6,703,950), "Gray Code Sequences."

***Conclusion***

**7**. Claims 7-11 are rejected as explained above.

**8**. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**9**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Sheng-Jen Tsai/
Partial Signatory Examiner, Art Unit 2186
March 10, 2008

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186
March 10, 2008